

IRF7507

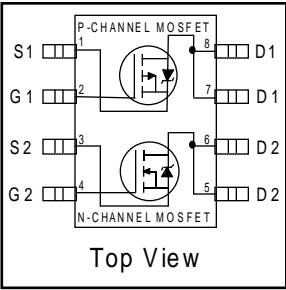
HEXFET® Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- Dual N and P Channel MOSFET
- Very Small SOIC Package
- Low Profile (<1.1mm)
- Available in Tape & Reel
- Fast Switching

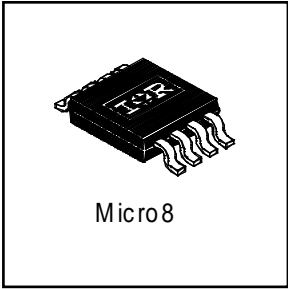
Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The new Micro8 package, with half the footprint area of the standard SO-8, provides the smallest footprint available in an SOIC outline. This makes the Micro8 an ideal device for applications where printed circuit board space is at a premium. The low profile (<1.1mm) of the Micro8 will allow it to fit easily into extremely thin application environments such as portable electronics and PCMCIA cards.



	N-Ch	P-Ch
V_{DS}	20V	-20V
$R_{DS(on)}$	0.135 Ω	0.27 Ω



Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
I_D @ $T_A = 25^{\circ}\text{C}$	Continuous Drain Current, V_{GS} @ 4.5V	2.4	-1.7	A
I_D @ $T_A = 70^{\circ}\text{C}$	Continuous Drain Current, V_{GS} @ 4.5V	1.9	-1.4	
I_{DM}	Pulsed Drain Current ①	14	-9.6	
P_D @ $T_A = 25^{\circ}\text{C}$	Power Dissipation	1.25		W
	Linear Derating Factor	10		mW/ $^{\circ}\text{C}$
V_{GS}	Gate-to-Source Voltage	± 12		V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	-5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150		$^{\circ}\text{C}$

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④	—	100	$^{\circ}\text{C}/\text{W}$

All Micro8 Data Sheets reflect improved Thermal Resistance, Power and Current -Handling Ratings- effective only for product marked with Date Code 505 or later .

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Unit	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
		P-Ch	-20	—	—		$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.041	—	$V/^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
		P-Ch	—	-0.012	—		Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	N-Ch	—	—	0.135	Ω	$V_{GS} = 4.5V, I_D = 1.7A$ ③
			—	—	0.20		$V_{GS} = 2.7V, I_D = 0.85A$ ③
			—	—	0.27		$V_{GS} = -4.5V, I_D = -1.2A$ ③
		P-Ch	—	—	0.40		$V_{GS} = -2.7V, I_D = -0.60A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	0.70	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		P-Ch	-0.70	—	—		$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	N-Ch	2.6	—	—	S	$V_{DS} = 10V, I_D = 0.85A$ ③
		P-Ch	1.3	—	—		$V_{DS} = -10V, I_D = -0.60A$ ③
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	1.0	μA	$V_{DS} = 16V, V_{GS} = 0V$
		P-Ch	—	—	-1.0		$V_{DS} = -16V, V_{GS} = 0V$
		N-Ch	—	—	25		$V_{DS} = 16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
		P-Ch	—	—	-25		$V_{DS} = -16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	N-P	—	—	± 100	nA	$V_{GS} = \pm 12V$
Q_g	Total Gate Charge	N-Ch	—	5.3	8.0	nC	N-Channel $I_D = 1.7A, V_{DS} = 16V, V_{GS} = 4.5V$ ③
		P-Ch	—	5.4	8.2		
Q_{gs}	Gate-to-Source Charge	N-Ch	—	0.84	1.3		P-Channel $I_D = -1.2A, V_{DS} = -16V, V_{GS} = -4.5V$
		P-Ch	—	0.96	1.4		
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	—	2.2	3.3	ns	N-Channel $V_{DD} = 10V, I_D = 1.7A, R_G = 6.0\Omega, R_D = 5.7\Omega$ ③
		P-Ch	—	2.4	3.6		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	5.7	—		P-Channel $V_{DD} = -10V, I_D = -1.2A, R_G = 6.0\Omega, R_D = 8.3\Omega$ ③
		P-Ch	—	9.1	—		
t_r	Rise Time	N-Ch	—	24	—	pF	N-Channel $V_{GS} = 0V, V_{DS} = 15V, f = 1.0\text{MHz}$ ③
		P-Ch	—	35	—		
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	15	—		
		P-Ch	—	38	—		
t_f	Fall Time	N-Ch	—	16	—	pF	P-Channel $V_{GS} = 0V, V_{DS} = -15V, f = 1.0\text{MHz}$ ③
		P-Ch	—	43	—		
C_{iss}	Input Capacitance	N-Ch	—	260	—		
		P-Ch	—	240	—		
C_{oss}	Output Capacitance	N-Ch	—	130	—	pF	N-Channel $V_{GS} = 0V, V_{DS} = 15V, f = 1.0\text{MHz}$ ③
		P-Ch	—	130	—		
C_{rss}	Reverse Transfer Capacitance	N-Ch	—	61	—		
		P-Ch	—	64	—		

Source-Drain Ratings and Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch	—	—	1.25	A	$T_J = 25^\circ\text{C}, I_S = 1.7A, V_{GS} = 0V$ ③
		P-Ch	—	—	-1.25		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	14		
		P-Ch	—	—	-9.6		
V_{SD}	Diode Forward Voltage	N-Ch	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 1.7A, V_{GS} = 0V$ ③
		P-Ch	—	—	-1.2		$T_J = 25^\circ\text{C}, I_S = -1.2A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	N-Ch	—	39	59	ns	N-Channel $T_J = 25^\circ\text{C}, I_F = 1.7A, di/dt = 100A/\mu s$ ③
		P-Ch	—	52	78		
Q_{rr}	Reverse Recovery Charge	N-Ch	—	37	56	nC	P-Channel $T_J = 25^\circ\text{C}, I_F = -1.2A, di/dt = 100A/\mu s$ ③
		P-Ch	—	63	95		

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 21)
- ② N-Channel $I_{SD} \leq 1.7A, di/dt \leq 66A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
P-Channel $I_{SD} \leq -1.2A, di/dt \leq 100A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
- ③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ④ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.

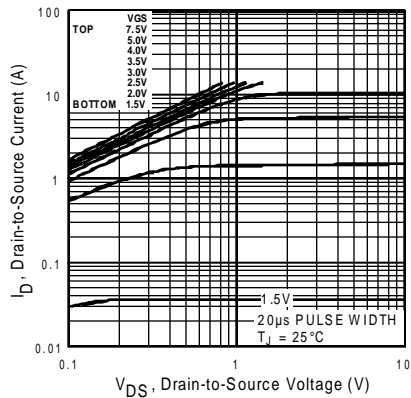


Fig 1. Typical Output Characteristics

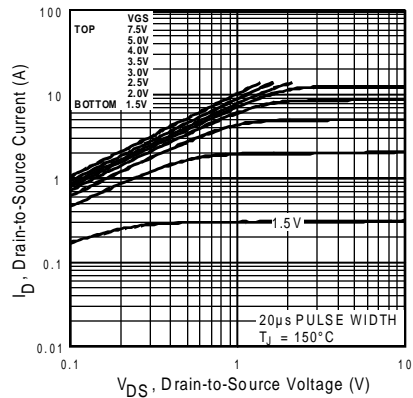


Fig 2. Typical Output Characteristics

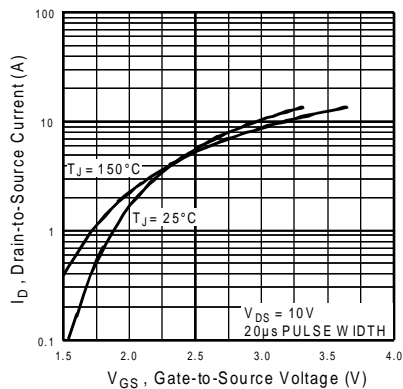


Fig 3. Typical Transfer Characteristics

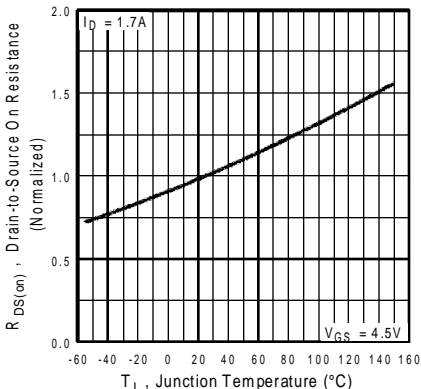


Fig 4. Normalized On-Resistance Vs. Temperature

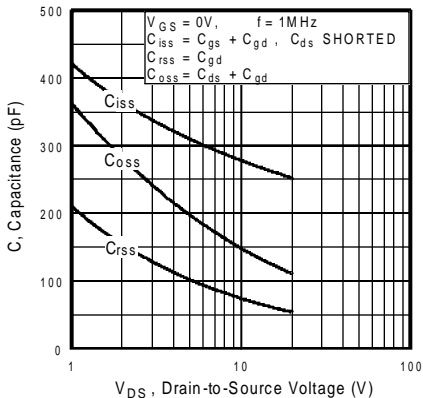


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

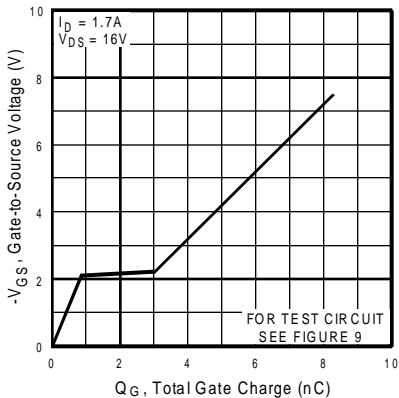


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

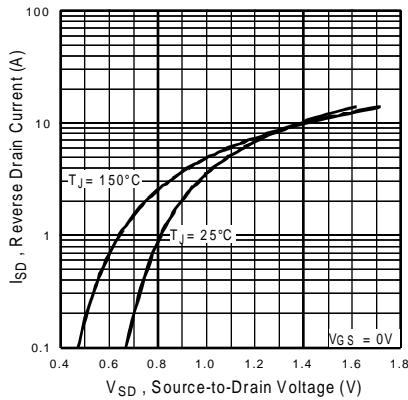


Fig 7. Typical Source-Drain Diode Forward Voltage

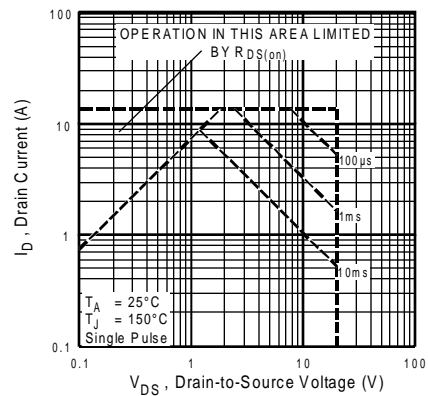


Fig 8. Maximum Safe Operating Area

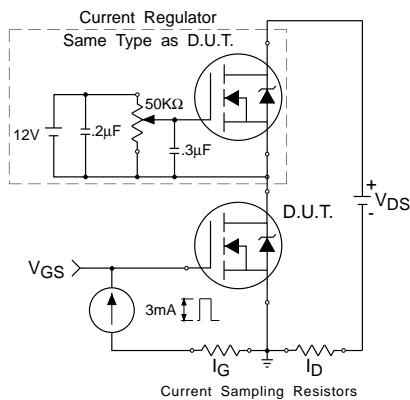


Fig 9a. Gate Charge Test Circuit

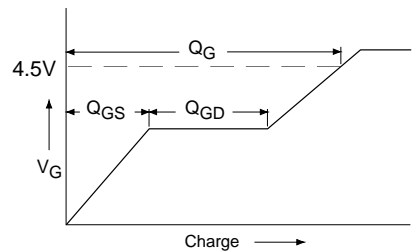


Fig 9b. Basic Gate Charge Waveform

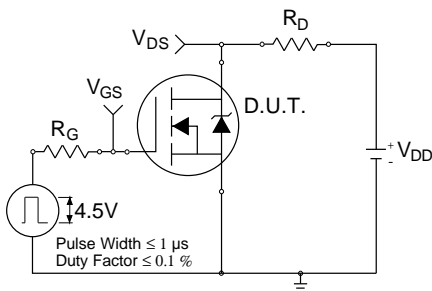


Fig 10a. Switching Time Test Circuit

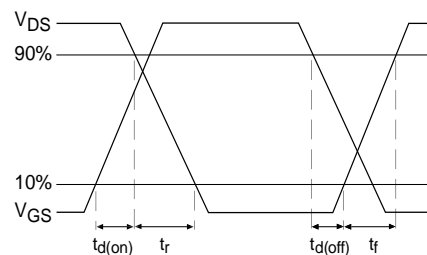
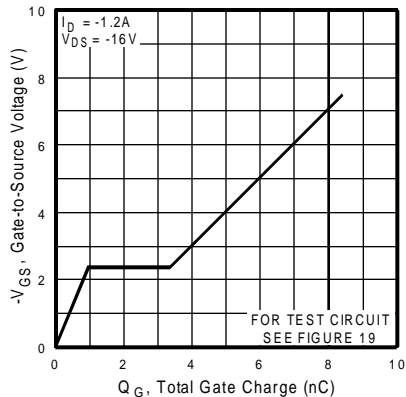
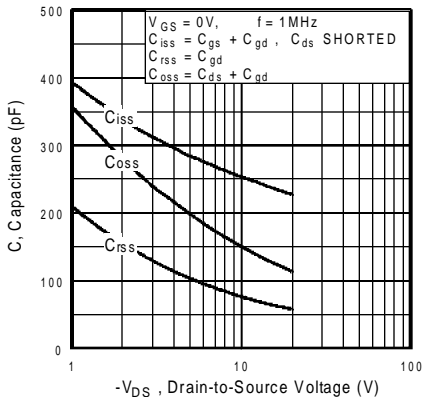
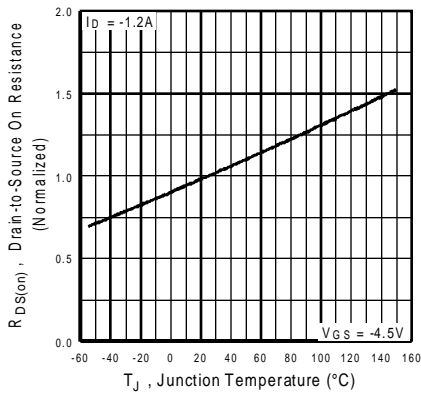
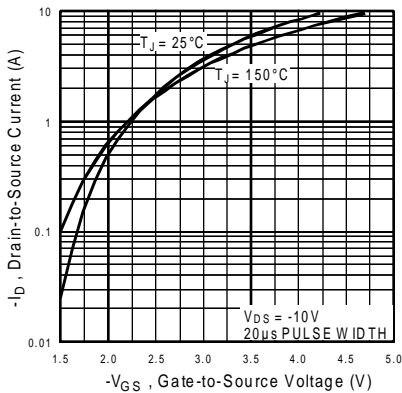
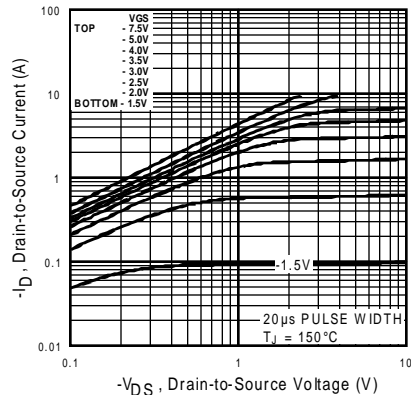
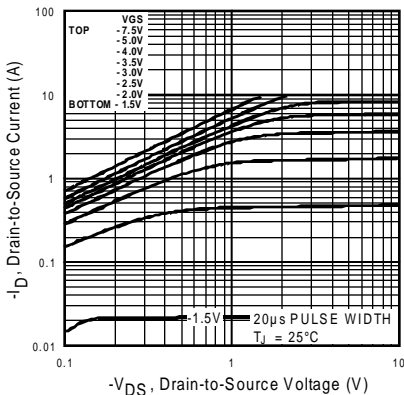


Fig 10b. Switching Time Waveforms



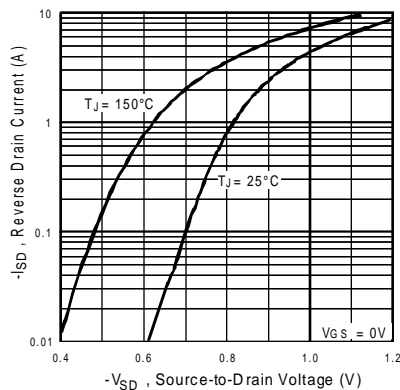


Fig 17. Typical Source-Drain Diode Forward Voltage

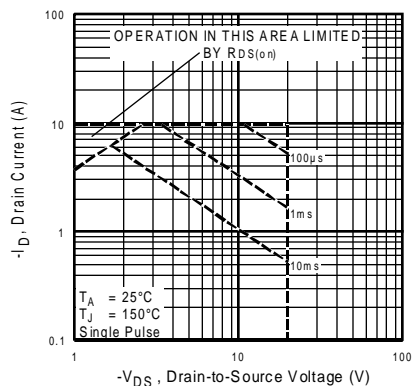


Fig 18. Maximum Safe Operating Area

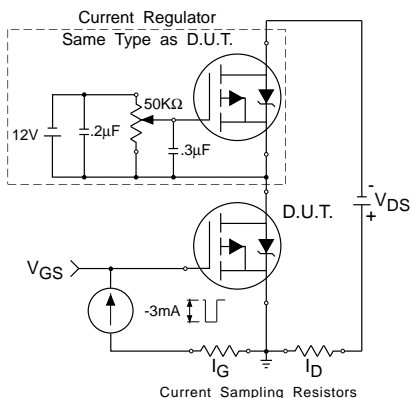


Fig 19a. Gate Charge Test Circuit

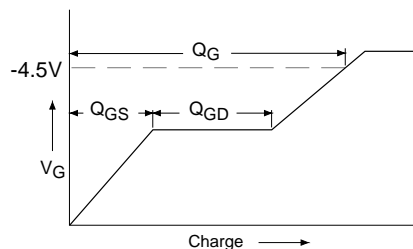


Fig 19b. Basic Gate Charge Waveform

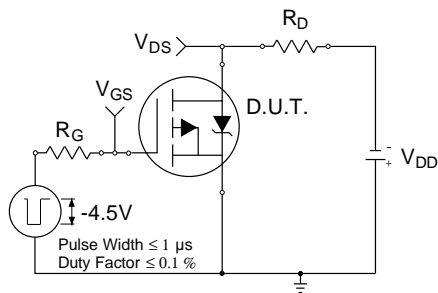


Fig 20a. Switching Time Test Circuit

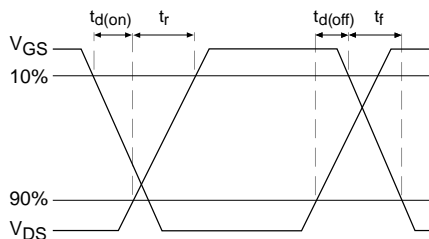


Fig 20b. Switching Time Waveforms

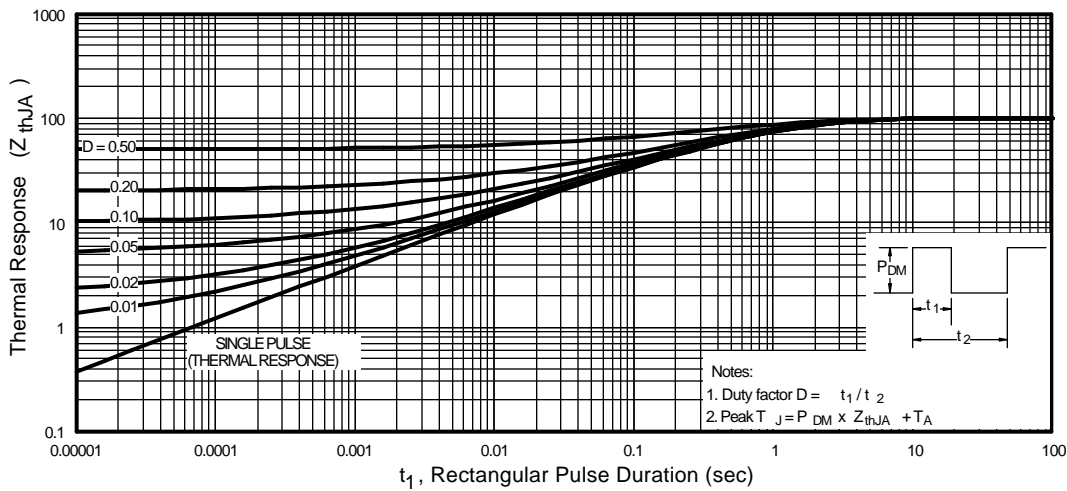


Fig 21. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

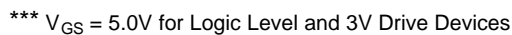
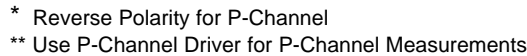
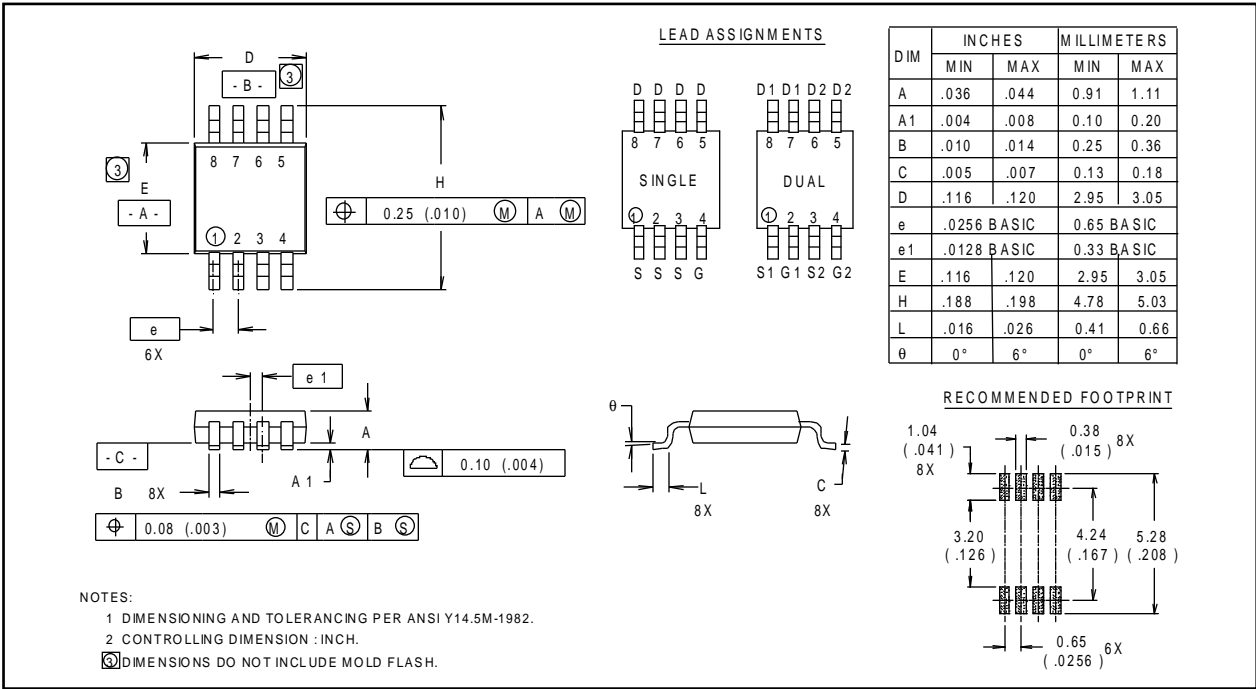


Fig 22. For N and P Channel HEXFETS

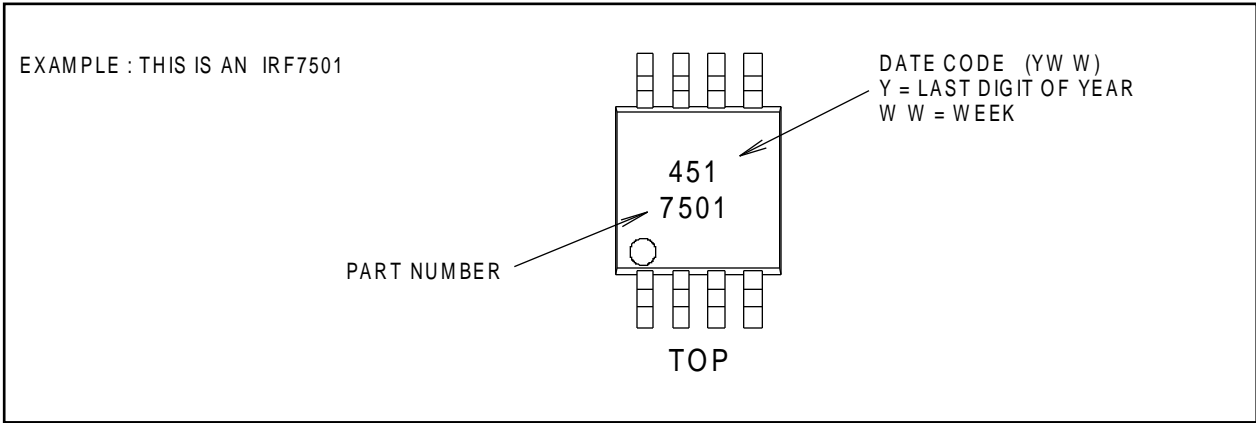
Micro8 Outline

Dimensions are shown in millimeters (inches)



Part Marking Information

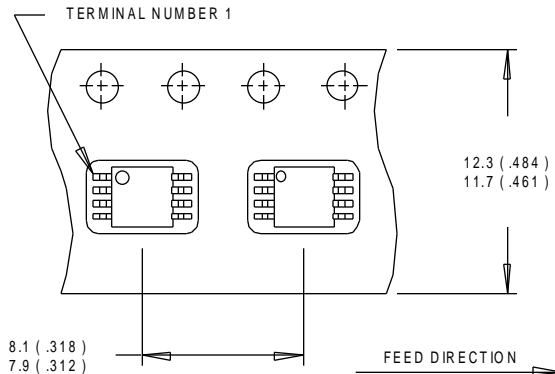
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Tape & Reel Information

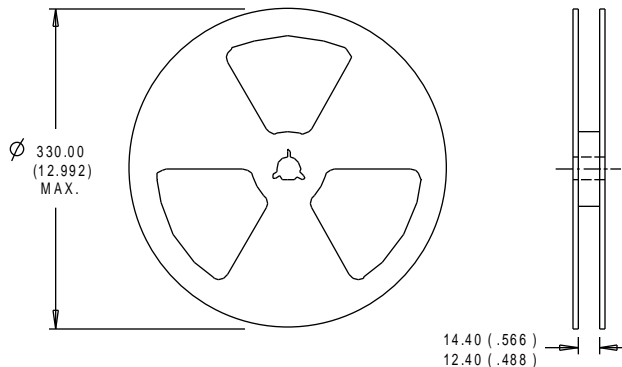
Micro8

Dimensions are shown in millimeters (inches)



NOTES:

1. OUTLINE CONFORMS TO EIA-481 & EIA-541.
2. CONTROLLING DIMENSION : MILLIMETER.



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.